

AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions, and listings, of claims in the application:

1           1.       (Currently Amended) A method, comprising:  
2           providing a semiconductor substrate;  
3           forming electrically conductive columns ~~[[on]]~~ over the semiconductor substrate;  
4           forming electrically conductive rows crossing ~~[[over]]~~ the electrically conductive  
5 columns;  
6           forming a plurality of memory components each having a resistance value corresponding  
7 to multiple logical bits; and  
8           forming non-volatile memory cells, each formed by connecting a memory component  
9 between an electrically conductive row and an electrically conductive column, wherein the  
10 non-volatile memory cells are formed without transistors for reduced space usage on the  
11 semiconductor substrate by each memory cell.

1           2.       (Currently Amended) ~~A method as recited in claim 1,~~ A method, comprising:  
2           providing a semiconductor substrate;  
3           forming electrically conductive columns over the semiconductor substrate;  
4           forming electrically conductive rows crossing the electrically conductive columns;  
5           forming a plurality of memory components each having a resistance value corresponding  
6 to multiple logical bits; and  
7           forming non-volatile memory cells, each formed by connecting a memory component  
8 between an electrically conductive row and an electrically conductive column,  
9           wherein ~~[[each]]~~ the memory component is components are formed to have ~~[[a]]~~ varying  
10 resistance value values based on a thickness at least one of: (1) varying thicknesses of  
11 electrically resistive material materials that forms an individual are part of respective memory  
12 component components; (2) varying areas of electrically resistive materials that are part of  
13 respective memory components; and (3) varying geometric shapes of electrically resistive  
14 materials that are part of respective memory components.

1           3.       (Original) A method as recited in claim 1, wherein each memory component is  
2       formed to have a resistance value based on an area of electrically resistive material that forms an  
3       individual memory component.

1           4.       (Original) A method as recited in claim 1, wherein each memory component is  
2       formed to have a resistance value based on a geometric shape of electrically resistive material  
3       that forms an individual memory component.

1           5.       (Original) A method as recited in claim 1, wherein the plurality of memory  
2       components are each formed to have a different resistance value based on a different area of  
3       electrically resistive material that forms a memory component.

1           6.       (Currently Amended) ~~A method as recited in claim 1,~~ A method, comprising:  
2       providing a semiconductor substrate;  
3       forming electrically conductive columns over the semiconductor substrate;  
4       forming electrically conductive rows crossing the electrically conductive columns;  
5       forming a plurality of memory components each having a resistance value corresponding  
6       to multiple logical bits; and  
7       forming non-volatile memory cells, each formed by connecting a memory component  
8       between an electrically conductive row and an electrically conductive column,

9       wherein the plurality of memory components are each formed to have a resistance value  
10      based on a rectangular geometric shape of electrically resistive material that forms a memory  
11      component, at least some of the rectangular geometric shapes having different resistance values  
12      corresponding to an area of a rectangular geometric shape.

1           7.     (Currently Amended) ~~A method as recited in claim 1,~~ A method, comprising:  
2                 providing a semiconductor substrate;  
3                 forming electrically conductive columns over the semiconductor substrate;  
4                 forming electrically conductive rows crossing the electrically conductive columns;  
5                 forming a plurality of memory components each having a resistance value corresponding  
6 to multiple logical bits; and  
7                 forming non-volatile memory cells, each formed by connecting a memory component  
8 between an electrically conductive row and an electrically conductive column,  
9                 wherein forming the non-volatile memory cells comprises:  
10                forming a first memory cell having a memory component that indicates logical bits 00  
11 (zero-zero);  
12                forming a second memory cell having a memory component that indicates logical bits 01  
13 (zero-one);  
14                forming a third memory cell having a memory component that indicates logical bits 10  
15 (one-zero); and  
16                forming a fourth memory cell having a memory component that indicates logical bits 11  
17 (one-one).

1           8.       (Currently Amended) ~~A method as recited in claim 1,~~ A method, comprising:  
2           providing a semiconductor substrate;  
3           forming electrically conductive columns over the semiconductor substrate;  
4           forming electrically conductive rows crossing the electrically conductive columns;  
5           forming a plurality of memory components each having a resistance value corresponding  
6           to multiple logical bits; and  
7           forming non-volatile memory cells, each formed by connecting a memory component  
8           between an electrically conductive row and an electrically conductive column,  
9           wherein forming the non-volatile memory cells comprises:  
10          forming a first memory cell that indicates logical bits 00 (zero-zero) corresponding to a  
11          first resistance value based on an area of electrically resistive material that forms a memory  
12          component in the first memory cell;  
13          forming a second memory cell that indicates logical bits 01 (zero-one) corresponding to a  
14          second resistance value based on an area of electrically resistive material that forms a memory  
15          component in the second memory cell;  
16          forming a third memory cell that indicates logical bits 10 (one-zero) corresponding to a  
17          third resistance value based on an area of electrically resistive material that forms a memory  
18          component in the third memory cell; and  
19          forming a fourth memory cell that indicates logical bits 11 (one-one) corresponding to a  
20          fourth resistance value based on an area of electrically resistive material that forms a memory  
21          component in the fourth memory cell.

1           9.       (Original) A method as recited in claim 1, wherein forming the plurality of  
2           memory components comprises forming individual memory components with a resistor in series  
3           with a diode.

1           10.      (Original) A method as recited in claim 1, further comprising configuring the  
2           resistance value of an individual memory component by exposing the memory component to  
3           light.

1           11.     (Original) A method as recited in claim 1, further comprising configuring the  
2 resistance value of an individual memory component by exposing electrically resistive material  
3 forming the memory component to light.

1           12.     (Original) A method as recited in claim 1, further comprising configuring the  
2 resistance value of an individual memory component by exposing the memory component to  
3 heat.

1           13.     (Original) A method as recited in claim 1, further comprising configuring the  
2 resistance value of an individual memory component by exposing electrically resistive material  
3 forming the memory component to heat.

1           14.     (Currently Amended) A method as recited in claim 1, wherein forming the non-  
2 volatile memory cells comprises:  
3           forming a first non-volatile memory cell by connecting a first memory component  
4 between an electrically conductive row and a first electrically conductive column, the first non-  
5 volatile memory cell formed as part of a first layer of non-volatile memory cells; and  
6           forming a second non-volatile memory cell by connecting a second memory component  
7 between the electrically conductive row and a second electrically conductive column, the second  
8 non-volatile memory cell formed as part of a second layer of non-volatile memory cells, the  
9 second layer formed over the first layer.

1           15. – 22. (Cancelled)

1           23.   (New) A method comprising:  
2           providing electrically conductive row traces and electrically conductive column traces;  
3           providing memory cells having respective resistive components, the resistive components  
4 connected between respective row and column traces without connecting through isolation  
5 circuitry,  
6           an individual one of the resistive components having a resistance value representing  
7 plural logical bits.

1           24.   (New) The method of claim 23, wherein providing the memory cells having  
2 respective resistive components connected between respective row and column traces without  
3 passing through isolation circuitry comprises providing the memory cells having respective  
4 resistive components connected between respective row and column traces without passing  
5 through transistors.

1           25.   (New) The method of claim 23, wherein providing the memory cells having  
2 respective resistive components connected between respective row and column traces without  
3 passing through isolation circuitry comprises providing the memory cells having respective  
4 resistive components connected between respective row and column traces without passing  
5 through transistors or diodes.

1           26.   (New) The method of claim 23, further comprising:  
2           connecting a selected one of the column traces to a first voltage;  
3           connecting a selected one of the row traces to a second voltage such that electrical current  
4 passes through a selected memory cell; and  
5           connecting unselected column and row traces to voltages generally equal to the first  
6 voltage to reduce parasitic electrical current through unselected memory cells.

1           27.   (New) The method of claim 26, wherein connecting the selected row trace to the  
2 second voltage comprises connecting the selected row trace to ground.

1           28.   (New) The method of claim 23, wherein providing the memory cells comprises  
2 providing the memory cells in at least a first layer and a second layer, the first layer being  
3 provided over the second layer.

1           29.   (New) The method of claim 23, wherein providing the memory cells having  
2 respective resistive components comprises providing resistive components having varying  
3 resistance values based on at least one of: (1) varying thicknesses of electrically resistive  
4 materials that are part of respective resistive components; (2) varying areas of electrically  
5 resistive materials that are part of respective resistive components; and (3) varying geometric  
6 shapes of electrically resistive materials that are part of respective resistive components.

1           30.   (New) The method of claim 1, wherein forming the non-volatile memory cells  
2 comprises connecting the memory components of respective memory cells between respective  
3 columns and rows without connecting through a transistor or diode.